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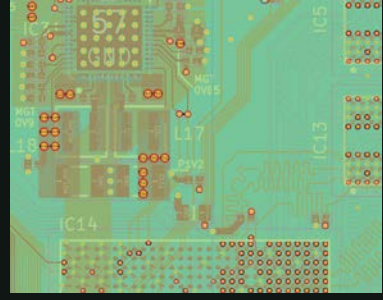
Design to Realization Quality

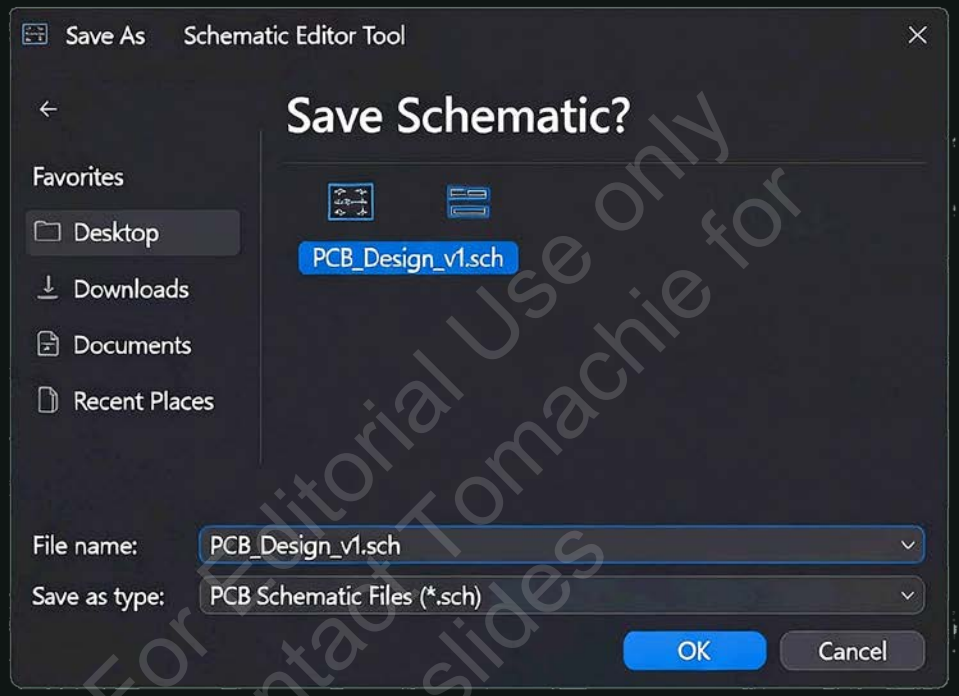
An AI-Assisted Automated Design Quality Baseline for PCB Development

CJ Clark, co-founder

Selected slides available for media/editorial use only
Contact Press-may2026@tomachie.com for clean slides

Reality





PCB test methodologies are permanently fixed when you click OK

Fault coverage: Unknown

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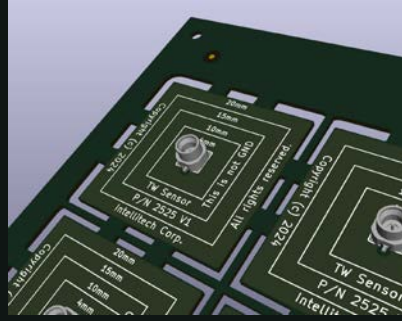
How it started: 30-Year Need



- PCB ATPG from an exported netlist imperfect
  - no pin names, is it digital/analog pin?
  - Requires adding in models
- Test program/Fixture developer brought in after first PCB is made – too late.
- Intellitech working towards “PCB test - right by construction” or “PCB test – correct first time”
- Need full data from native cad tool

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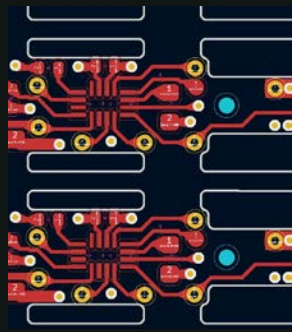
How It’s going



- AI Assisted PCB design analysis
- Automated Design Quality baseline at schematic freeze
- Clear documentation and checklists for PCB realization
- Fault coverage across ATE, AXI, AOI
- Intelligent Test Point Insertion before layout

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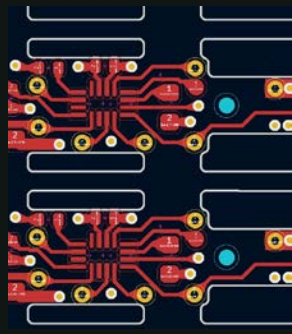
How its going



- AI Assi
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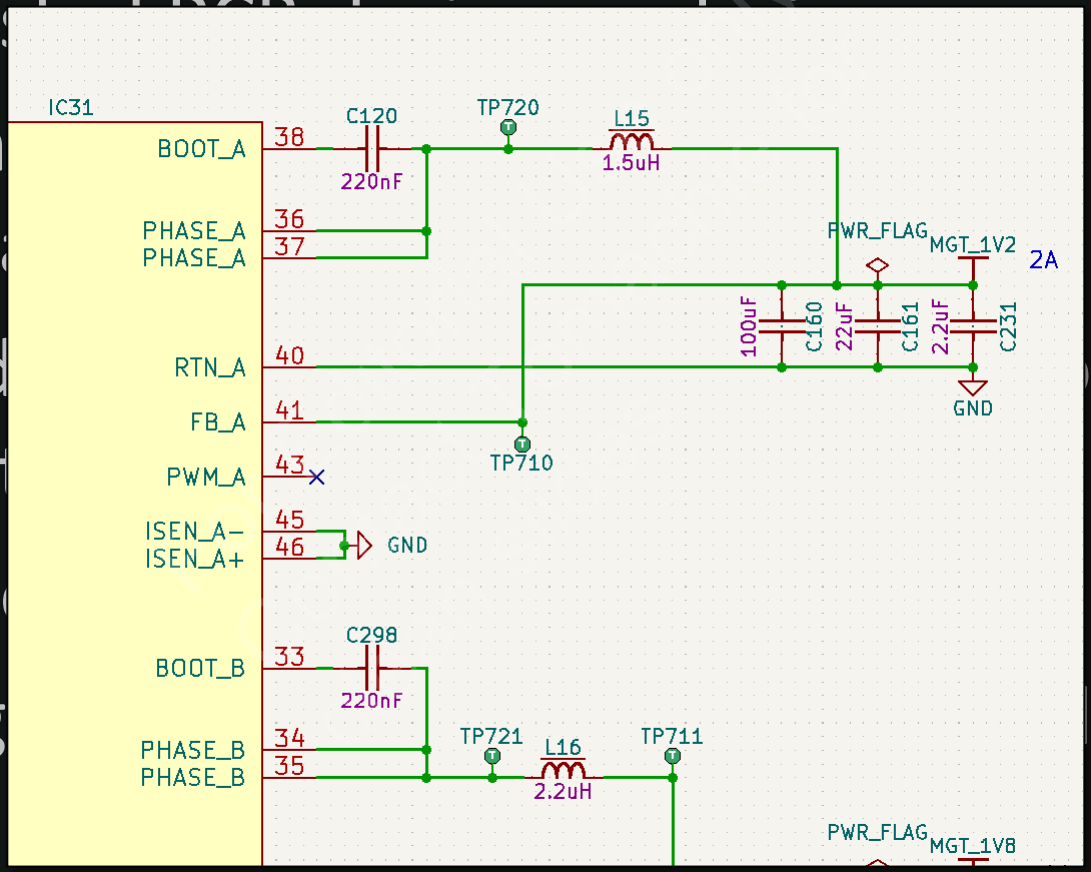
- Intellig



r PCB

layout

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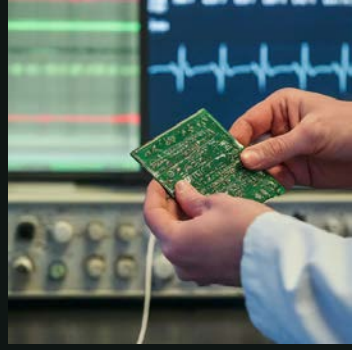
“I feel your pain”

- US President Bill Clinton



- 21 years of software with integrated hardware product realization for PCB test
- IC design to shuttle-fab service experience
- PCB design experience (latest Kicad 2024)
- IEEE 1149.1/JTAG chairperson (twice), IEEE 1149.10 (SERDES/spi/i2c) chair/editor
- CEO Intellitech Corp/ hands-on engineering management

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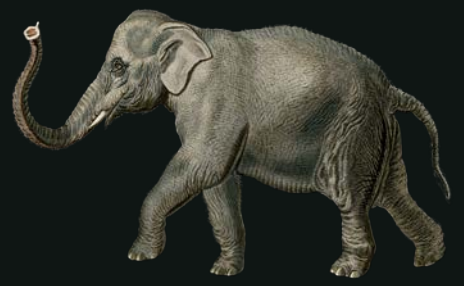
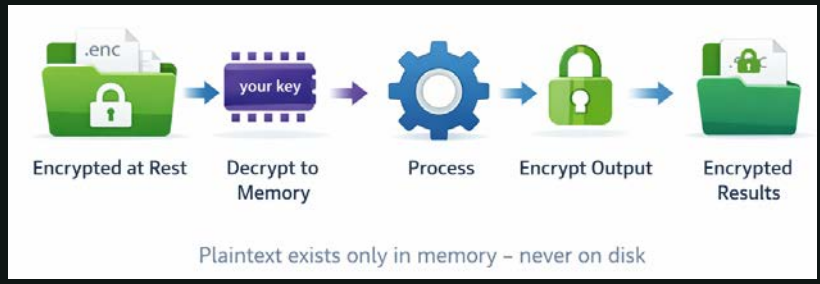
Addressing the Elephant: Design Confidentiality

https://www.tomachie.com/pcb-private-encryption.html



- 25 years of handling confidential schematics across all industries — trusted by professionals
- Tomachie hosted in SOC 2 Type II certified data center
- Uploads are all protected via HTTPS/TLS 1.2
  - Same as your banking information
- CDA/NDA agreement signing available upon request
- Need Zero knowledge?
  - AES-256 Private Encryption for EIP
  - Uses OpenSSL
  - Security review available
- Potentially design is more secure than current contractor methods



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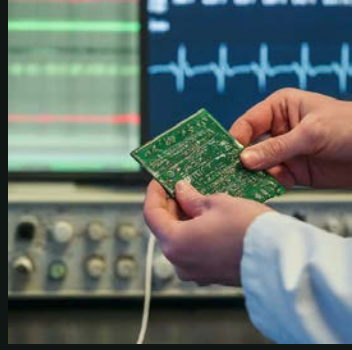
Design Intent, Made Externally Auditable



- Tomachie exposes design intent outside the CAD tool
- Artifacts designed for review, audit, and trust
- Pinout Documents and metrics for non-technical stakeholders
- Test Coverage – early on – time to focus on functional test and ATE test strategy

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Why Early Matters

- By layout or fabrication, access and test coverage are fixed
- Late-stage tools discover problems after decisions are irreversible
- Tomachie operates when quality is still a design choice

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Design for Accountability

- Used where designs are reviewed, questioned, and audited
- Supports handoff to test, manufacturing, and external partners
- Creates evidence with details that survive beyond the PDF schematic

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The “NC” ambiguity

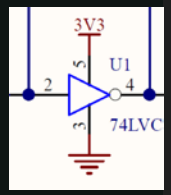
Library quality checks show incomplete library models
Substituted part – functionally equivalent – NC meant “don’t connect anything to this pin”. NC pin 1 hidden in library behind pin 2 caused short on PCB.

Grade D (poor)	2 (9.1%)
Grade F (fail)	19 (86.4%)
OVERALL LIBRARY QUALITY	F (0.27/4.00)

14.2 Component Library Validation

Checking for generic/incomplete library models using statistical patterns.

Library Model Issues (23 models)						
Library Name	**Industry Name**	**Part Number**	**RefDes**	**Pins**	**Distribution**	**Issues**
74LVC1G04SE	-	-	U1, U2	5	P:5	Pin 1 (NC) at same location as pin 2 (A); All pins marked as Passive - likely generic library model; No Power pins - may use separate power symbol; Only 1 pin type used - no electrical differentiation; Power-named pins not typed as Power - library pin types incomplete [GND=Passive, VCC=Passive]



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Output Enable Checks

13.3 Oscillator OE Test Points

Certain production PCB tests require oscillators to be turned off. OE pins require pull resistors with test points to achieve that.

Oscillator	Type	Issue
X2	OSC_25M_NZ2520SB	EN has pull-up resistor but no test point at R5_2, X2_1
X1	OSC_24M_NZ2520SB	EN has pull-up resistor but no test point at R4_2, X1_1

13.4 IC Enable Test Point Check

ICs with enable pins (power switches, regulators, etc.) require test points for fixture-based test to disable the device during test.

IC	Type	Pin Name	Pin #	Issue
U7	LD39050P	EN	1	EN tied to VCC - recommend pull-up resistor and test point
U16	STMPS2141STR	$\overline{\text{EN}}$	4	$\overline{\text{EN}}$ has pull-up resistor but no test point at R116_1, R117_2, U16_4 - Active-low enable with pull-up disables output when pin 4 is not driven.
U10	STLD40DPUR	EN	7	EN has pull-up resistor but no test point at R81_1, R85_1, U10_7

- Next step – automatic fix: insert TP and pull resistor

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Why the Correct value Field matters!

Test generation/BOM/pick-place need the correct value in a predictable place

2 Component Value Properties

Component values should be in the VALUE property, either as a direct value (e.g. 100nF) or as a formula reference (e.g. =Capacitance). Both methods are accepted by Altium. The typed property (Resistance, Capacitance, Inductance, Impedance, etc.) holds the actual electrical value; VALUE should point to it or contain the same data.

Value Property Check

Type	Check	Count	Components	Status
Capacitors	VALUE references Capacitance (e.g. C5107 Capacitance=100.0 nF)	1282	C5107, C5106, C5111, C5113, C5114, C5108, C5100, C5101 (+1274 more)	✓
Resistors	VALUE references Resistance (e.g. R5101 Resistance=0.0 Ohm)	946	R5101, R5100, R5102, R5103, R5108, R5109, R5110, R5111 (+938 more)	✓
Resistors	Values in VALUE or Resistance	144	R5133, R5205, R4907, R4908, R4909, R4935, R4924, R4915 (+136 more)	✓
Resistors	VALUE blank but Resistance property exists (e.g. R5309 Resistance=61.9 Ohm, VALUE should be =Resistance)	36	R5309, R5310, R5320, R5319, R5330, R5329, R5432, R5434 (+28 more)	✗
Inductors	VALUE references Inductance (e.g. L5300 Inductance=100.0uH)	78	L5300, L5301, L5303, L5302, L5305, L5304, L4901, L4903 (+70 more)	✓

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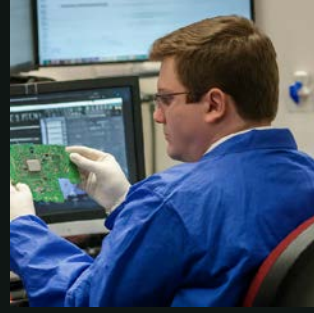
Hierarchical correctness checks



3.3 Unconnected Off-Sheet Ports

1 pin(s) with off-sheet connector that doesn't connect anywhere:

Refdes_Pin	Pin Function	Pin Property	Device Type	Net Name	Notes
U7900_6	1A2	Passive	74AVC4T245	PCIE-WAKE_3V3	Entry: PCIE-WAKE_3V3

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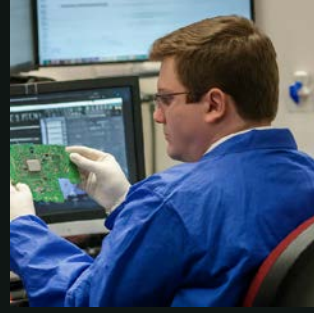
EMC shield and logic GND checks



EMC Check Summary		
Check	**Issues**	**Status**
Connector Shell Grounding	3	✗

12.1 Connector Shell Grounding

RefDes	Type	Issue	Recommendation	Severity
CN13	USB-MICRO-AB	CN13: Shield pins Shield connected directly to digital GND. Shell currents should not couple into the digital ground plane.	Create net CHASSIS (or your company standard name). Move ALL shell pins to CHASSIS. Add ONE explicit connection from CHASSIS to digital GND (visible on schematic, preferably near power entry or at this connector) using: a) 0-ohm resistor (most common), b) ferrite bead, or c) 1000 pF - 0.01 uF capacitor (optionally with 1 Mohm bleed resistor in parallel).	✗

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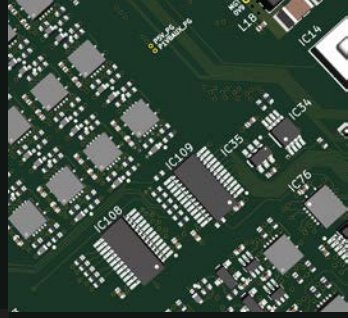
LSSI construction checks

Low-Speed Serial Interfaces (i2c, SWD, JTAG, SPI, SPMI etc)



I2C Pull-up Check			
Net	**Component**	**Status**	
SDA		Pull-up on SDA was not detected. A pull-up for basic I2C operation would be about 4.7K ohms. Even if an IC has internal pull-ups on its inputs, they are likely just for biasing the input high (47-100K ohms) and are not sufficient for I2C. We did not consult the datasheet for U2 but low-value resistors cost silicon area, so it is unlikely the IC has them.	✗
SCL		Pull-up on SCL was not detected. A pull-up for basic I2C operation would be about 4.7K ohms. Even if an IC has internal pull-ups on its inputs, they are likely just for biasing the input high (47-100K ohms) and are not sufficient for I2C. We did not consult the datasheet for U2 but low-value resistors cost silicon area, so it is unlikely the IC has them.	✗
SDA1	R51	Pull-up resistor 4.7K (R51) found on SDA	✓
SCL1	R49	Pull-up resistor 4.7K (R49) found on SCL	✓
SDA2	R56	Pull-up resistor 4.7K (R56) found on SDA	✓

13.6 Boundary Scan Testability

The BSDL for U1 (ATSAM3X8EA-AU) specifies JTAGSEL be asserted to logic 1 and TST be asserted to logic 0 for IEEE 1149.1 compliance. U1_46 JTAGSEL is tied to GND. Consider adding a TestPoint and a soft pull-down such that the TAP selection can be controlled for debug and production test.

13.6.1 BSDL Identification

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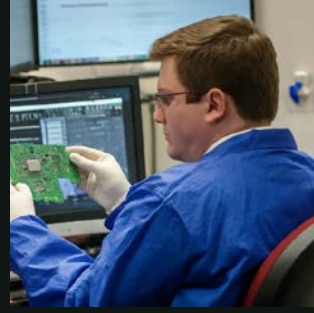
Design for Manufacturability and Test – at the schematic phase



- AXI/AOI equipment/ATE/ATPG and other processes rely on compliant footprint naming

1.3 Footprint Compliance

Production pick-n-place, AOI, AXI, ATE and Design Quality tools rely on proper descriptions of component footprints.

Footprint Naming	Status
21 SMT footprints do not follow IPC-7351B naming	✗
8 footprints (connectors, specialty) — compliance unknown	
4 footprints could not be classified for inspection	✗

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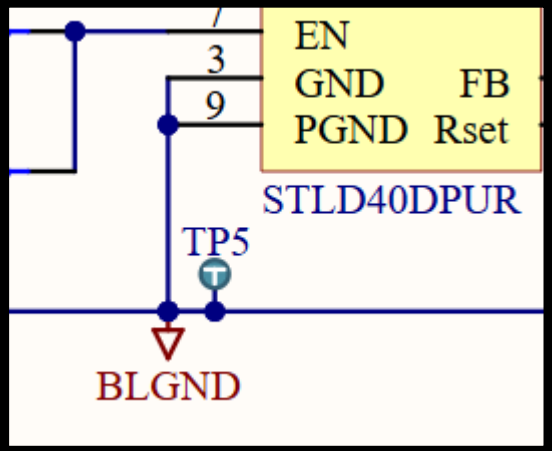
Intelligent TP insertion



Multi-process fault-coverage

Real world, no-spin fault-coverage from AI
- (guided by experienced PCB test pros that design and build assembled PCBs)

13.9.2 Per-Pin Fault Coverage Matrix

● = Detected ◐ = Partially detected - = Not tested | E = Electrical (ICT/flying probe) O = Optical (AOI) X = X-ray (AXI)

Pin ⇅	Net ⇅	E Opens ⇅	E Shorts ⇅	O Opens ⇅	O Shorts ⇅	X Opens ⇅	X Shorts ⇅
U5_N3	PA0	●	●	-	-	●	◐
U5_H15	PC6	●	●	-	-	●	◐
U5_N4	DCMI_HSYNC	●	●	-	-	●	◐
U5_P3	DCMI_PIXCK	●	●	-	-	●	◐
U5_G15	PC7	●	●	-	-	●	◐
U5_G14	uSD_D0	●	●	-	-	●	◐
U5_B14	uSD_D2	●	●	-	-	●	◐

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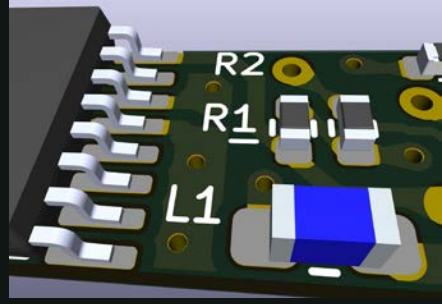
Something for everyone



- Enables design teams to establish a clear schematic quality baseline
  - No guess work on “Do I need a TP here?”
  - Saves engineering time / reduces downstream friction
- Documented quality for internal/external non-technical customer review
- Clear win for production & ATE team
- Lowers cost at EMS

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When will you get your first checkmark?

- Upload your own Altium, KiCad (or soon OrCAD) schematic ZIP at www.tomachie.com
- Enter your email
- Try the free sample designs from Texas Instruments, ST Microelectronics & others
- Instant HTML report with all the checks, tables, fault coverage
- Download updated schematics with test-point s
- Complimentary analysis available starting May 1, 2026
- **During embargo, credentialed media use key: GOMAY**