Orthogone

Developers of the
Seemingly Impossible

PRODUCT BRIEF

LICENSABLE
INTELLECTUAL
PROPERTY
FOR FPGA, ASIC OR
ASSP DESIGNS

ULL PCIe DMA Controller

APPLICATIONS

- Electronic Trading
- Networking
- Storage
- Security
- High Performance Computing (HPC)

MOVE DATA FASTER BETWEEN FPGA-BASED SmartNIC AND HOST CPU.

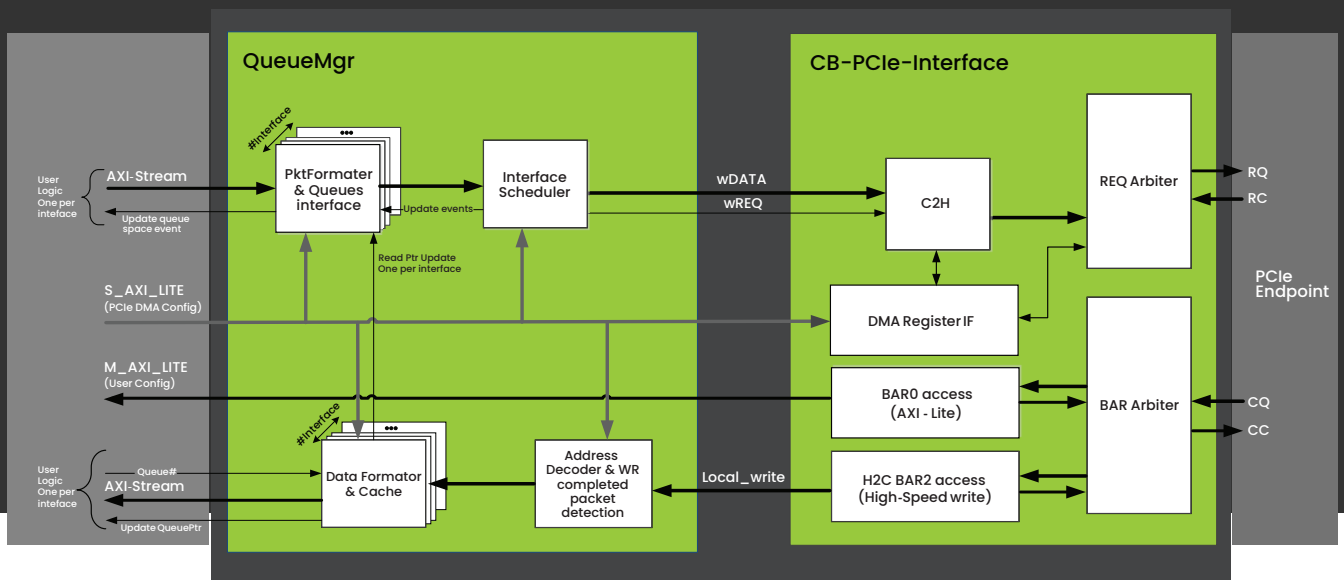
The **ULL PCIe DMA Controller** implements bidirectional data transfer between the host CPU and FPGA through a PCIe interface with a round-trip time under 640ns. This IP core features multiple build time parameters, allowing the users to efficiently design their applications while maximizing resource utilization without compromising latency performances.

In the **card-to-host direction**, packets are transferred through PCIe from FPGA to host buffer memory in separate memory blocks, one or many blocks depending on the packet size. In the **host-to-card path**, packets are transferred directly to the FPGA memory space through optimized PCIe transactions. Cut-through techniques are used to optimize latency to move data and control/status messages across the PCIe link.

Users get an array of features: **highly parameterizable IP core**, seamless **FPGA logic integration**, and comprehensive software development kit. Moreover, the package includes encrypted source code, simulation models, and comprehensive documentation.

ULL PCIe DMA Controller

HIGH-LEVEL BLOCK DIAGRAM



DELIVERABLES

- **Encrypted source code**
- **Reference design**
- **Simulation model**
- **Linux kernel module user space driver and libraries**
- **Product documentation**

Contact us for a personalized evaluation and to discuss the best way to try our products.

sales@orthogone.com

FEATURES*

- Highly parametrizable IP Core:
  - Number of channels
  - Number of queues per channel
  - Memory size of each queue
  - Interfaces AXI-4 Stream bus width and synchronous or asynchronous to PCIe clock
- Fully integrated with AMD/Xilinx PCIe Endpoint (up to Gen 4 x8)
- Easy integration with Orthogone TCP/IP and UDP/IP network stacks
- Standard AXI-4 streaming interfaces for seamless integration with FPGA logic
- Highly efficient FPGA implementation with low resources utilization
- High timing margin on -2 and -3 Xilinx/AMD UltraScale+ FPGA
- Designed explicitly for Kernel-bypass Linux applications that require ultra-low latency performances
- Polling and Ring Buffer DMA architecture
- Linux kernel module provided with standard delivery packages (rpm, deb)
- Driver created to automatically detect PCIe card for early evaluation solution
- Library API easily handles buffer creation, transmission and reception

PERFORMANCES OVERVIEW EXAMPLE*

Hardware Platform	PCIe	Payload Size	Core clock	RTT Latency
AMD x3522pv	Gen. 4 (x8)	32B	250MHz	644ns

- RTT min latency
- PCIe Gen4 x 8 lanes, Xilinx/AMD x3522pv, Intel(R) Xeon(R) Gold 5315Y CPU @ 3.20GHz.
- Synchronous AXI-4 Interfaces (512b, 250MHz)
- Payload counts: 128k

* *Information subject to change without notice.*

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