Orthogone
Developers of the Seemingly Impossible

FPGA Solutions

for Ultra-Low Latency SmartNIC

Designed for financial applications, network and compute acceleration

What is OT - ULL FPGA Framework

Hardware and **software** development framework

The **ULL FPGA framework** is a high-performance FPGA and software solution specifically designed for ultra-low latency networking applications and primarily for high-performance financial applications.

It provides users with the ability to quickly develop a broad portfolio of FPGA applications and gain a competitive edge by processing large amounts of data with near zero latency.

The framework features a full suite of FPGA IP cores implementing offload engines specifically designed for ultra-low latency networking applications.

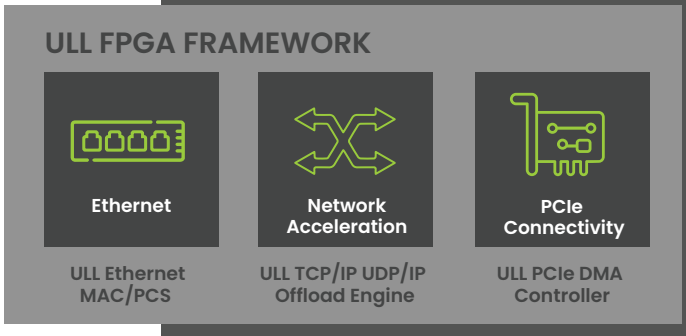
Typical use cases

- **Tick-to-trade electronic trading**
- **Smart order routers**
- **Pre-trade risk check engines**
- **Exchange interconnects**

Who should use Orthogone's Framework?

The performance offered by our ULL FPGA Framework is ideal for skilled developers of FPGA intensive fintech applications where latency is critical.

Primarily conceived for building high-performance financial applications, it can easily be adapted to design acceleration solutions for High-Performance Computing (HPC), data analytics, networking and security workloads.



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Solution details

Complete suite of ULL FPGA IP Cores

All FPGA IP cores achieve extremely low latency performance while maintaining a reasonable timing margin and preserving critical FPGA resources for on-chip computational acceleration.

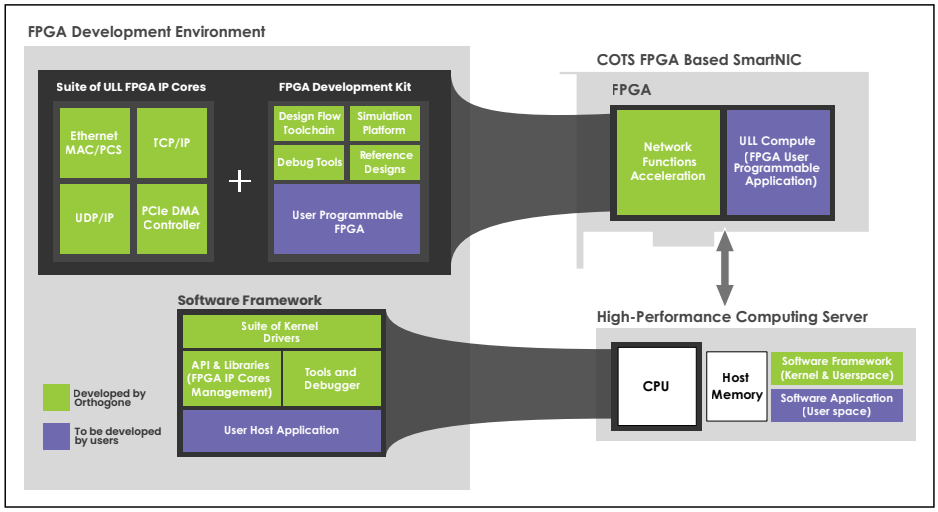
Development environment and reference design

A comprehensive FPGA development environment including design scripts, end-to-end simulation test benches, a AMD Alveo x3522pv reference design, and a complete suite of Linux drivers, libraries & API, and utility tools are provided to simplify and accelerate project development.

Flexibility and scalability

With its standard interfaces and highly customizable FPGA cores, the framework can easily support the addition of features and evolve according to your needs while maintaining exceptional performance.

Orthogone ULL FPGA Framework Solution



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Specifications

Ultra Low-Latency IP cores:

- **ULL-MAC/PCS core**
  (SoP-to-SoP - 37 ns RTT including GTY + MAC/PCS/CDC)
  Hardware acceleration for Ethernet packets
- **ULL-TCP / UDP core**
  (SoP-to-SoP 6.2 ns Tx)
  Hardware acceleration for TCP/IP and UDP/IP protocols
- **ULL-CBDMA core**
  Low-latency Circular Buffer DMA controller to move data extreme fast between SmartNIC and Host

Key benefits

- Full RTL implementation supporting layers 2, 3, 4 (ARP, IPv4, ICMP, TCP, UDP)
- Comprehensive FPGA development and simulation environments
- Highly parameterizable to meet the specific needs of each application
- AMD Alveo x3522pv reference design examples
- Complete suite of Linux drivers, libraries & API

Pricing model and support

Several pricing options are available depending on your needs and the platforms you use. We know how to adapt to your project and budget.

Contact us for more information on our licensing options.

Orthogone

Orthogone offers highly specialized engineering solutions focused on the design of innovative products requiring in-depth knowledge of software development, embedded systems and FPGAs.

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